

## Power Device Interface Controller Compatible with IEEE 802.3af/at Integrated Power MOSFET V1.2

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### Overview

XS2103S provides a complete interface for Power Devices (PD) in Ethernet Power over Ethernet (PoE) systems compliant with the IEEE802.3af/at standard. It offers detection signals, classification signals, and an integrated isolated power switch with surge current control. During surge events, XS2103S limits the current within 180 mA until the isolated power MOSFET is fully turned on, at which point it switches to a higher current limit from 760 mA to 1100 mA. The device features input undervoltage lockout (UVLO) with a wide hysteresis and long-duration pulse shielding to compensate for resistive losses in twisted-pair cables, ensuring interference-free transmission during power-on and power-off. XS2103S can withstand input voltages up to 100V.

XS2103S supports the two-event classification method of IEEE 802.3 at standard. The device detects the connection status of a wall adapter power source, enabling seamless switching from PoE power to wall adapter power. Additionally, XS2103S provides a power good (PG) signal, two levels of current limiting, and fold-back thermal protection, along with di/dt limiting. XS2103S is housed in a SOP8 package and operates over an extended temperature range of -40 °C to +105 °C.

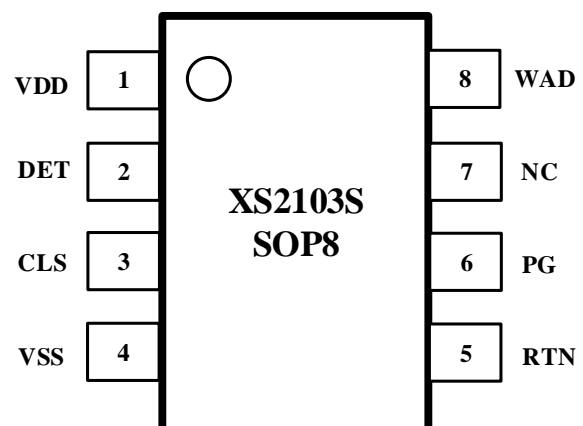
### Typical Application

- ◆ IP camera
- ◆ VoIP
- ◆ Wireless AP

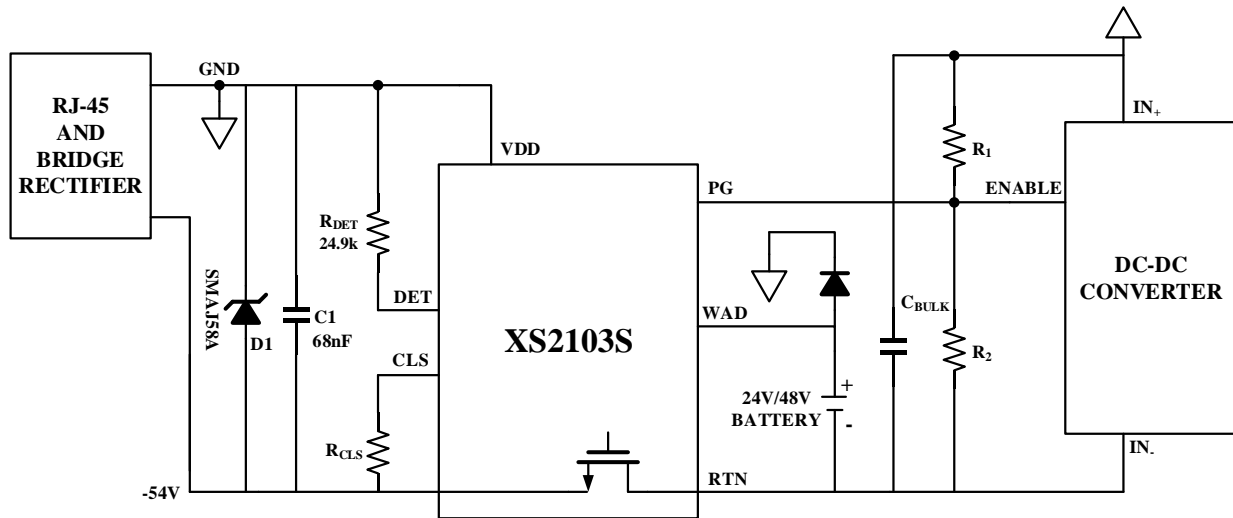
### Features

- ◆ Compatible with IEEE 802.3af/at
- ◆ Two-event classification
- ◆ Easy-to-use wall adapter interface
- ◆ PoE classification 0 to 4
- ◆ Absolute maximum input rating of 100 V
- ◆ Maximum surge current limit of 180 mA
- ◆ Normal operating current limit between 760 mA and 1100 mA
- ◆ Current limiting and fold-back protection
- ◆ Compatible with IEEE 802.3af/at and 39V UVLO
- ◆ Over temperature protection
- ◆ SOP-8 packaging

### Pin Configuration



Typical Application Diagram



Pin Description

Pin	Name	Features
1	VDD	Positive power input. Connect a bypass capacitor of 68 nF (minimum) between VDD and VSS.
2	DET	Detection resistor input. Connect a characteristic resistor ( $R_{DET} = 24.9 \text{ k}\Omega$ ) between DET and VDD.
3	CLS	Classification resistor input. Connect a resistor ( $R_{CLS}$ ) between CLS and VSS to set the required classification current. For specific PD classification corresponding resistor values, refer to the classification current indicators in Table 1.
4	VSS	Negative supply input. VSS is connected to the source of the integrated isolated N-channel power MOSFET.
5	RTN	Drain of the isolated MOSFET. Connect RTN to the downstream DC/DC converter ground as shown in the typical application circuit.
6	PG	Power-good open-drain output. When the hot-swap MOSFET is turning on, PG sinks current of 230 $\mu\text{A}$ to keep the downstream DC/DC converter off until the hot-swap switch is fully on. In detect, classify, and regulated supply modes, prevent PG from drawing current.
7	NC	NC
8	WAD	Wall adapter detector input. Enables wall adapter detection when VDD - VSS exceeds the event threshold. Detection occurs when the voltage between WAD and RTN exceeds 9V. Disconnects isolated N-channel power MOSFET and disables classification feature when a wall adapter is connected. Connect WAD directly to RTN when not using a wall adapter or other auxiliary power.